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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/605,293	06/28/2000	DAVID L. CHAPEK	MIO-0037-VA	5927

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EXAMINER	
RICHARDS, N DREW	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 09/11/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/605,293	Applicant(s) CHAPEK, DAVID L.	
	Examiner N. Drew Richards	Art Unit 2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 June 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-12 and 14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-12 and 14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 June 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. In view of the Appeal Brief filed on 6/17/2002, PROSECUTION IS HEREBY REOPENED. New grounds of rejection are set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

2. The issues raised for the first time in this Office Action should have been raised previously but were inadvertently overlooked. The examiner regrets any inconvenience this might cause.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the source, drain, and gate all formed **in** the semiconductor substrate must be shown or the feature(s) canceled from the claim(s). Also, the semiconductor substrate, layer of silicon dioxide on the semiconductor substrate, and the layer of polycrystalline silicon on the silicon

dioxide layer with the source, drain, and gate formed on the semiconductor substrate must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

4. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: The specification does not provide proper antecedent basis for a source, drain, and gate formed **in** the semiconductor substrate.

5. The specification is objected to for not complying with 35 U.S.C. 112, first paragraph. The specification has not been written so as to enable a person of ordinary skill in the art to form a source and drain in a substrate where the substrate comprises silicon dioxide, quartz, or glass. See page 10 lines 22-25 of the specification.

The specification also has not been written so as to enable a person of ordinary skill in the art to form a layer of polycrystalline silicon on silicon dioxide by thermal oxidation. See page 8 line 12, page 9 line 21, page 13 line 21 and page 14 line 15.

6. The disclosure is objected to because of the following informalities: Page 13 line 2 should refer to figure 5 instead of figure 3.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

8. Claim 10 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 10 recites a source, drain, and gate formed **in** the semiconductor substrate. The specification does not enable a gate formed in the substrate and the figures do not show a gate formed in the substrate. The specification does mention the gate formed in the substrate on page 10 line 25 but does not depict the gate in the substrate in figure 2 nor does the substrate give adequate description for forming a gate in the substrate to enable one of ordinary skill in the art to form the gate in the substrate.

9. Claims 11 and 12 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly

connected, to make and/or use the invention. Claims 11 and 12 claim a memory array and a semiconductor wafer, respectively. The claims include limitations claiming a layer of polycrystalline silicon over the silicon dioxide and a further gate, source and drain formed on the semiconductor substrate. This is not enabled as the only transistor disclosed in the memory array or semiconductor wafer (where the multiple transistors are formed on the substrate) is the transistor shown in figure 2, which does not have a source, drain, and gate formed on the semiconductor substrate. The only embodiment disclosed having a source, drain, and gate formed on the substrate is shown in figure 5 (the thin film transistor) but the embodiment of figure 5 is not enabled in a memory array or a wafer with a repeating series of gates, sources, and drains.

10. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

11. Claim 10 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 10 recites a layer of polycrystalline silicon formed on the silicon dioxide and later recites a gate formed in the substrate. It is unclear whether the layer of polycrystalline silicon recited is the same layer as the gate. Also, it is unclear whether the claimed silicon dioxide layer is the gate oxide layer 54 of figure 2 or the substrate as the specification describes the substrate being made of silicon dioxide and does not state what the gate oxide comprises beyond calling it a gate oxide.

12. As best understood, the claims are rejected as follows.

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art.

Applicant's admitted prior art discloses on page 1 lines 12-16 a semiconductor substrate, a layer of silicon dioxide on the substrate, and a layer of polycrystalline silicon formed on the silicon dioxide, the polycrystalline silicon having a smooth morphology. The admitted prior art discloses the layer of silicon dioxide having been doped with hydrogen ions. The semiconductor substrate is considered as a bottom portion of the silicon dioxide layer with the remaining silicon dioxide layer as the silicon dioxide layer upon the substrate. Though the admitted prior art does not explicitly state a layer of polysilicon is on the silicon dioxide it is implicitly understood that the polysilicon is formed seeing that the admitted prior art discusses performing the hydrogen doping of the silicon dioxide so as to provide a thinner, smoother polysilicon film deposited on the

silicon dioxide. The admitted prior art of lines 16-22 does not teach the layer of silicon dioxide being free of metal contaminants as the Kaufman ion source causes metal contaminants in the layer. The admitted prior art teaches the metal contaminants being produced from metal sputtering off a metal grid in the Kaufman ion source apparatus and that as device sizes decrease the effect of the damage from the metal contaminants increases.

Applicant's admitted prior art on page 1 line 23 through page 2 line 21 teaches the use of plasma source ion implantation. It teaches the PSII to dope semiconductors and various materials without using a metal grid. It would have been obvious to one or ordinary skill in the art at the time of the invention to use plasma source ion implantation to implant the hydrogen ions. The motivation for doing so is to provide a layer with increased surface hardness and improved optical properties as well as avoiding metal impurities.

Further, since the admitted prior art recognized the source of the metal contamination as the metal grid in the Kaufman ion source, it would have been obvious to one of ordinary skill in the art to perform the hydrogen implanting using a different apparatus that did not contain a metal grid. This would require only routine substitution of one known equivalent technique for another. The substitution of one known equivalent technique for another may be obvious even if the prior art does not expressly suggest the substitution. *Ex parte Novak* 16 USPQ 2d 2041 (BPAI 1989); *In re Mostovych* 144 USPQ 38 (CCPA 1964) ; *In re Leshin* 125 USPQ 416 (CCPA 1960) ;

Graver Tank & Manufacturing Co. v. Linde Air Products Co. 85 USPQ 328 (USSC 1950).

15. Claims 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burns et al. (Principles of Electronic Circuits, Pp. 380 and 381) in view of Applicant's admitted prior art.

Burns et al. teach a field effect transistor in figure 9.8 on page 381. Burns et al. teach a substrate, silicon dioxide layer, a layer of polycrystalline silicon over the silicon dioxide layer forming a gate, a source and a drain in the substrate. Burns et al. do not teach the layer of silicon dioxide having hydrogen ions implanted therein or being free of metal contaminants. Applicant's admitted prior art teaches implanting hydrogen ions into silicon dioxide on page 1 lines 12-16. Applicant's admitted prior art as combined above, also teaches using plasma source ion implantation on page 1 line 23 through page 2 line 21 to implant the hydrogen ions which results is the silicon dioxide being free of metal contaminants.

Burns et al. and Applicant's admitted prior art are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to implant hydrogen ions into the silicon dioxide layer. The motivation for doing so is to prepare the surface of the silicon dioxide for the deposition of a layer of polycrystalline silicon to provide for a thinner and smoother polycrystalline silicon film. Further, at the time of the invention it would have been obvious to a person of ordinary skill in the art to implant the hydrogen atoms by

plasma source ion implantation. The motivation for doing so is to provide a layer with increased surface hardness and improved optical properties as well as avoiding metal impurities. Therefore, it would have been obvious to combine Burns et al. with Applicant's admitted prior art to obtain the invention of claim 10.

With regard to claim 11, Burns et al. teach on pages 380 and 381, a memory array which further includes a plurality of memory cells arranged in rows and columns comprising at least one field effect transistor having a gate source and drain formed on the substrate.

With regard to claim 12, Official Notice is taken that one of ordinary skill in the art at the time of the invention would form the transistor of claim 10 or the memory array of claim 11 on a semiconductor wafer including a plurality of die. This is well known as in semiconductor processing multiple devices are formed on a single wafer then split into individual die to allow for processing of a great number of die at one time to save of processing costs.

16. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Murata et al. (U.S. Patent No. 5576229) in view of Applicant's admitted prior art.

Murata et al. teach a thin film transistor in figure 6E comprising a semiconductor substrate of glass, a layer of polycrystalline silicon 507 formed on a portion of the substrate, a insulating layer 503 formed on a portion of the polycrystalline silicon, a source region 507a and drain region 507b formed in the polycrystalline silicon, and a gate electrode 504 formed on the insulating layer. Murata et al. do not teach the

substrate having hydrogen ions implanted therein or the substrate being free of metal contaminants. Applicant's admitted prior art teaches implanting hydrogen ions into a silicon dioxide (glass) layer to provide a smooth topology polycrystalline silicon film thereon on page 1 lines 12-16. Applicant's admitted prior art, as combined above, also teaches using plasma source ion implantation on page 1 line 23 through page 2 line 21 to implant the hydrogen ions which results is the silicon dioxide (glass) being free of metal contaminants.

Murata et al. and Applicant's admitted prior art are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to implant hydrogen ions into the glass substrate. The motivation for doing so is to prepare the surface of the glass substrate for the deposition of a layer of polycrystalline silicon to provide for a thinner and smoother polycrystalline silicon film. Further, at the time of the invention it would have been obvious to a person of ordinary skill in the art to implant the hydrogen atoms by plasma source ion implantation. The motivation for doing so is to provide a layer with increased surface hardness and improved optical properties as well as avoiding metal impurities. Therefore, it would have been obvious to combine Murata et al. with Applicant's admitted prior art to obtain the invention of claim 14.

Response to Arguments

17. Applicant's arguments filed 6/24/02 have been fully considered but they are not persuasive.

Applicant has argued that the admitted prior art is not properly combinable to reject claim 9 because the admitted prior art lacks proper motivation for the combination. Applicant states that the motivation must be found in the prior art and not based on the applicant's disclosure. The motivation in this case comes from the prior art, the admitted prior art, and not from the applicant's disclosure of the invention. The "disclosure" which cannot be used for the motivation is the disclosure of the invention, including the summary of the invention, the detailed description, and the claims. The background section, which includes admitted prior art, is permissible as a source of motivation. In the case law cited by applicant, the motivation used did not come from any of the references applied in the rejection but rather came from the applicant's disclosure. That is different from this case as the motivation for the current rejections comes straight from one of the applied references, the admitted prior art.

Applicant also argued that they do not admit that the prior art of record recognized the problem of metal contamination when using a Kaufman ion source. This is not persuasive as the applicant states in the background section of the application that the Kaufman ion source contaminates the target object. The background section is taken as admitted prior art.

Applicant also argues that the Examiner has made an incorrect assertion in asserting that the admitted prior art teaches the use of PSII to implant which results in the silicon dioxide layer being free of metal contaminants. This assertion is deemed correct. It has been shown that it is obvious to use PSII to implant the hydrogen. The result of this step is a silicon dioxide layer free of contaminants.

Applicant also argue that providing a layer with increased surface hardness and improved optical properties cannot be proper motivation because the claimed invention does not require these properties. This is not persuasive because the fact that applicant has recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. See *Ex parte Obiaya*, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to N. Drew Richards whose telephone number is (703) 306-5946. The examiner can normally be reached on M-F 8:00-5:30; Every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

NDR
August 29, 2002

EDDIE LEE
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